UNIVERSITY OF BIRMINGHAM | SCHOOL OF PHYSICS AND ASTRONOMY

Pixel detectors: from segmented diodes to monolithic imaging sensors

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Particle Physics Seminar

8 November 2017

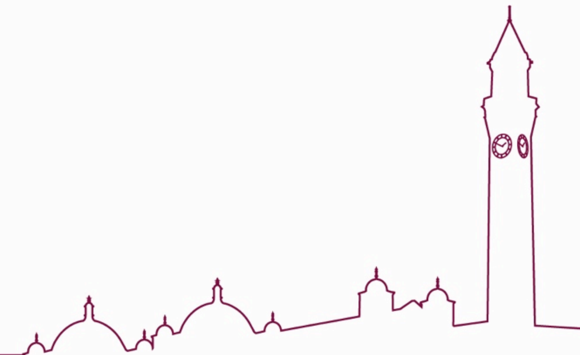
Outline

- Segmented silicon detectors for tracking and vertexing

- State-of-the art pixel detectors
  - Hybrid pixel detectors
  - Monolithic Active Pixel Sensors (MAPS)

- New developments
  - Depleted MAPS
  - Digital electromagnetic calorimetry with DMAPS at future colliders

- Conclusion

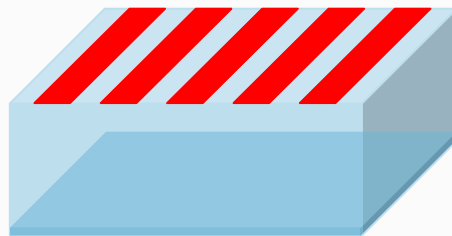


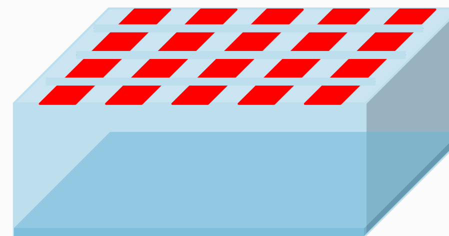
Segmented silicon detectors

- Highly segmented silicon detectors have been used in particle and nuclear physics experiments for over 40 years
  - Technology of choice for **tracking and vertex detectors**
  - They detect the passage of ionizing radiation with good spatial resolution and efficiency

- The success of silicon detectors is due both to **semiconductor properties** and evolution of **silicon fabrication technology**

- They consist of a sensing element (i.e. **sensor**) with its associated **readout electronics**

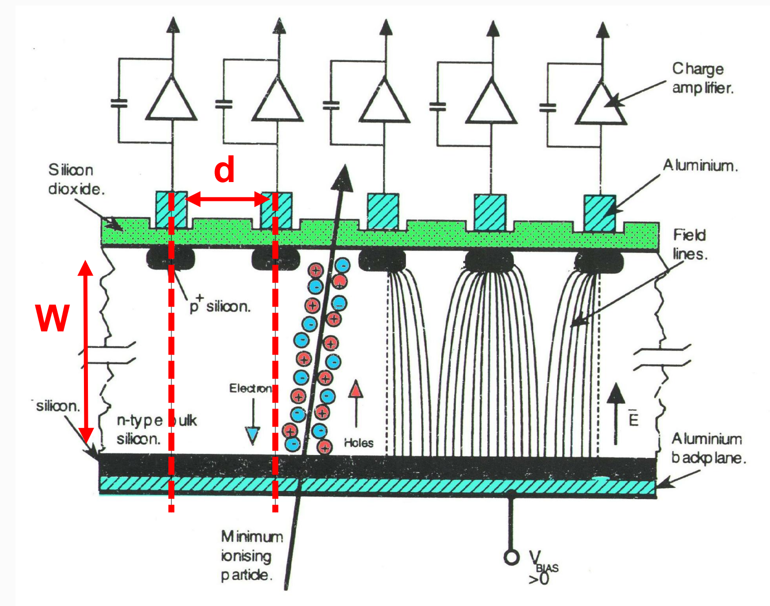

Strip sensor


Pixel sensor

Sensor working principle

- Silicon sensors work as a **reverse biased pn-junction (i.e. diode)**
  - **High resistivity** silicon bulk
  - Highly doped contacts
- The segmentation (pitch, d) defines the **spatial resolution** (σ)
- **High (reverse) bias voltage** (V_{bias})
  - **Depletion**
  - Electric field

Cross section of a silicon sensor

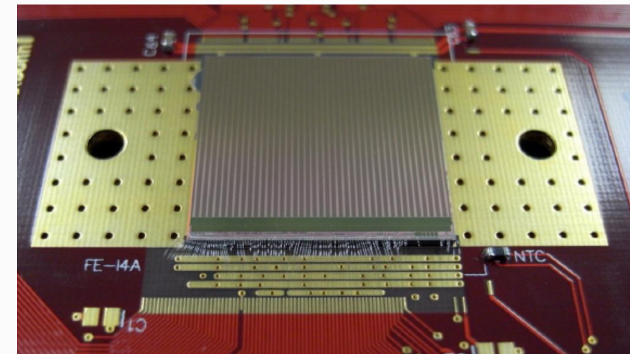


$$W \propto \sqrt{\rho V_{bias}}$$

- Traversing charged particles create e-/h+ pairs
- Movement of charges (i.e. **drift** in electric field) towards the electrodes generates a signal

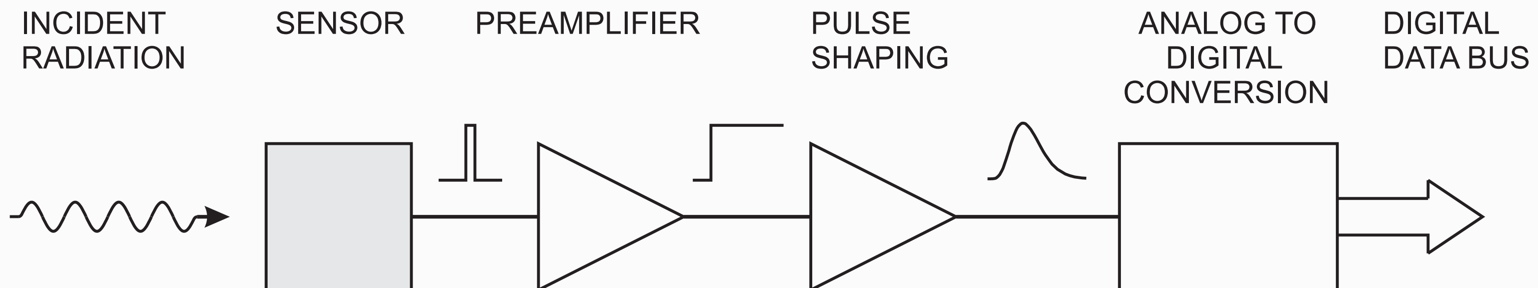
Basics of readout electronics

ATLAS FE-I4 readout ASIC



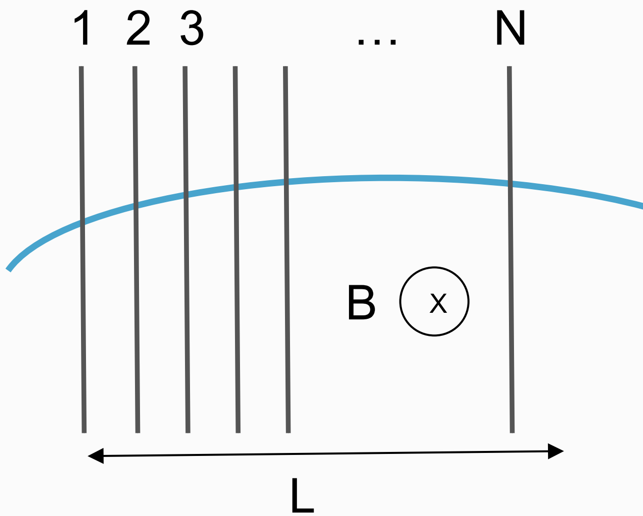
- Mixed-mode Application Specific Integrated Circuits (**ASIC**) in deep submicron **CMOS technologies**

- Signal processing functions per readout channel
  - 1 readout channel per pixel
  - Amplification and pulse shaping
  - Analogue to digital conversion (for example comparator with threshold)



H. Spieler, Semiconductor Detector Systems, Oxford University Press

Tracking and momentum resolution



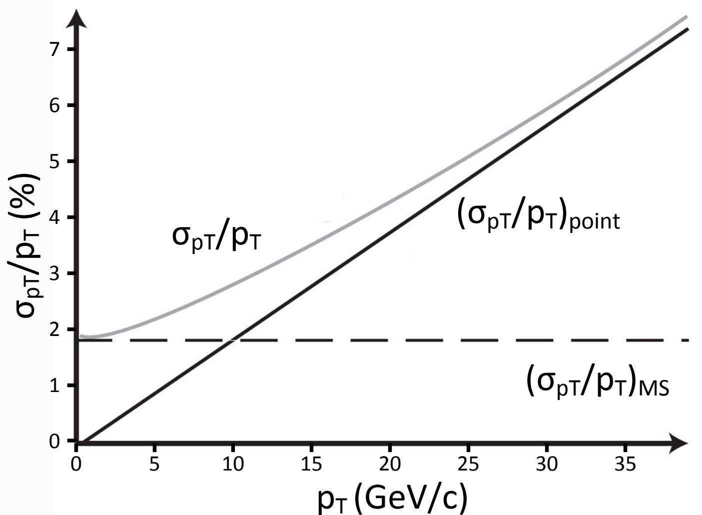
$$\frac{\sigma_{p_T}}{p_T} = \sqrt{\left(\frac{\sigma_{p_T}}{p_T}\right)^2_{point} + \left(\frac{\sigma_{p_T}}{p_T}\right)^2_{MS}}$$

Point resolution

$$\left(\frac{\sigma_{p_T}}{p_T}\right)_{point} = p_T \cdot \frac{\sigma}{0.3BL^2} \cdot \sqrt{\frac{720N^3}{(N-1)(N+1)(N+2)(N+3)}}$$

Multiple scattering term

$$\left(\frac{\sigma_{p_T}}{p_T}\right)_{MS} = \frac{1}{0.3B}\frac{0.0136}{\beta}\sqrt{\frac{C_N}{LX_0}}$$



Detector requirements

- Fine segmentation
- Large detector
- Low material

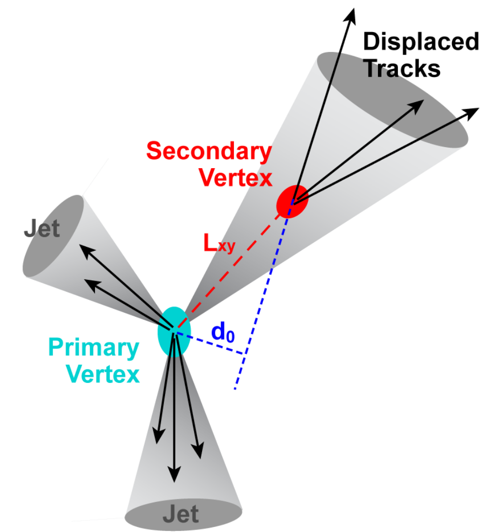
Vertex resolution

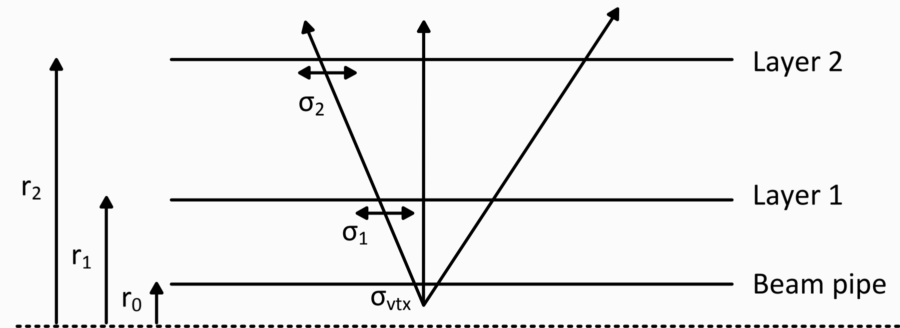
- Vertex resolution

$$\sigma_{vtx} = \sqrt{\left(\frac{r_1}{r_2 - r_1} + 1\right)^2 \sigma^2 + (2r_1 - r_0)^2 (13.6\,\mathrm{MeV})^2 \frac{x}{X_0} \frac{1}{p^2}}$$

- Impact parameter resolution

$$\frac{13.6\mathrm{MeV}}{\beta p} \sqrt{x/X_0}$$





Detector requirements

- Fine segmentation
- Low material (beam pipe and detector layers)
- First layer as close as possible to the beam pipe
- Large lever arm

Challenges: high rate or high precision

- Physics and experimental conditions drive the detector requirements
  - Granularity, radii and number of layers, readout electronics, material budget, …

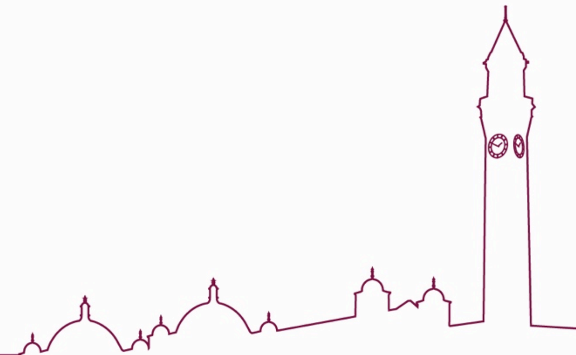
- **High rate** experiments
  - Proton-proton colliders
  - **Radiation hardness of sensor and ASIC**
  - Fast collection of large charge in the sensor
  - High **memory density** and data throughput in ASIC

  → **Hybrid** pixel detectors

- **High precision** experiments
  - e+/e- colliders and heavy Ions (HI) experiments
  - High **spatial resolution**
  - **Thin detectors**

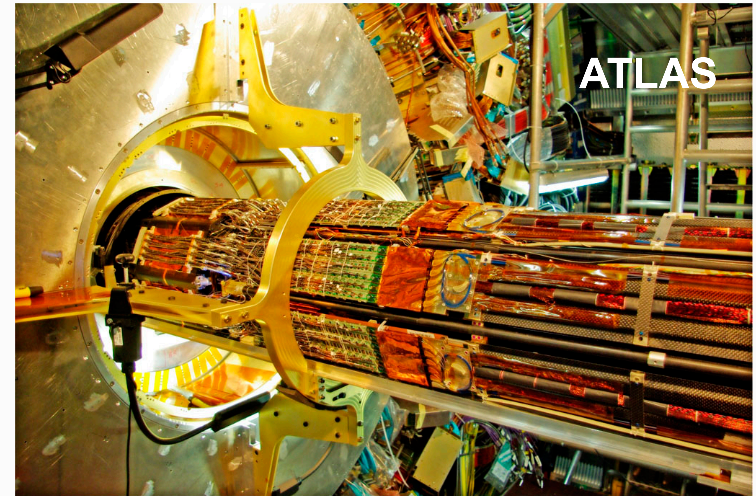
  → **Monolithic Active Pixel Sensors**

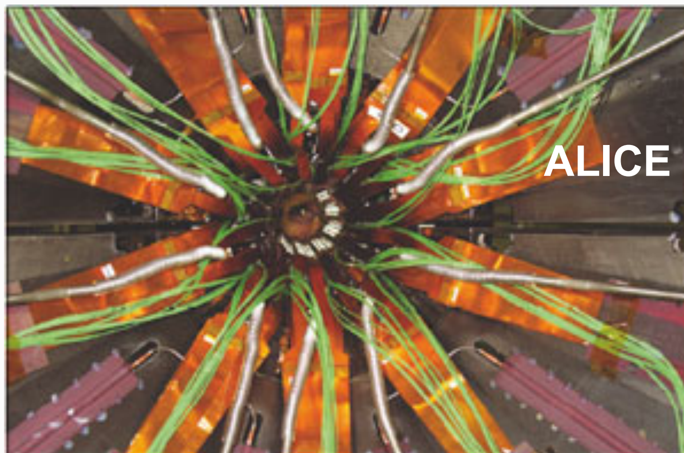
State-of-the art pixel detectors: Hybrid pixel detectors

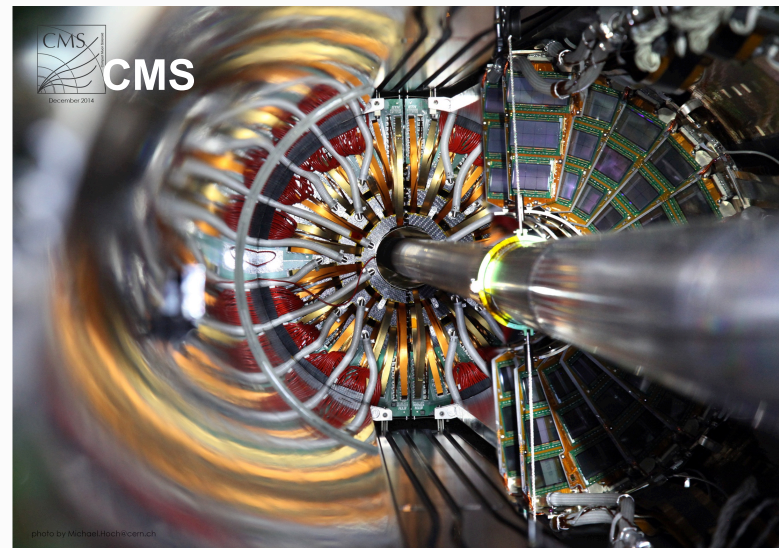


Hybrid pixel detectors in HEP

- **ATLAS, CMS and ALICE** use hybrid pixel detectors close to the interaction point
  - Complemented by strip detectors at large radii
- Largest pixel systems ever built in HEP (**~m²**)

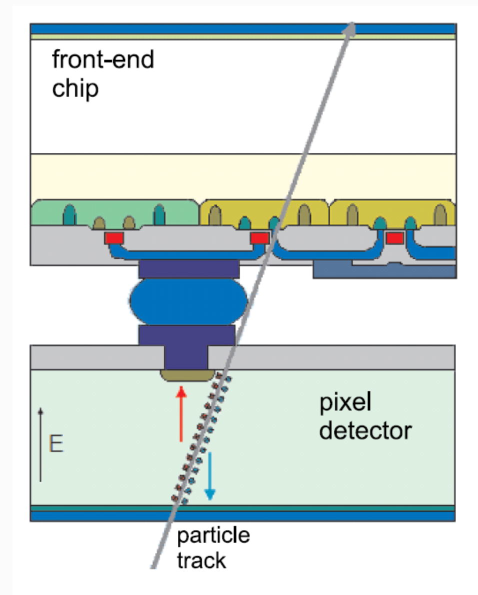


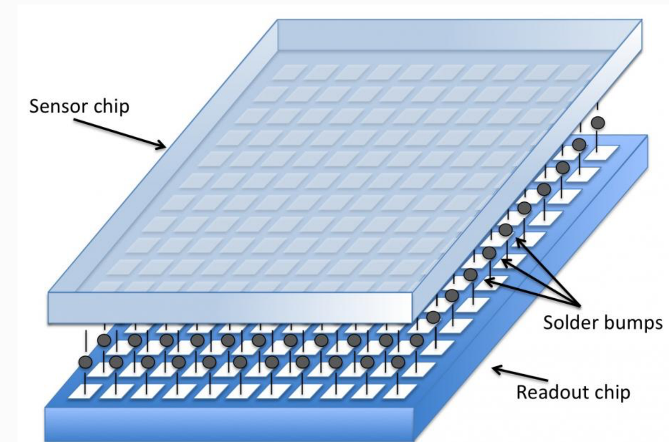




Hybrid pixel detector concept

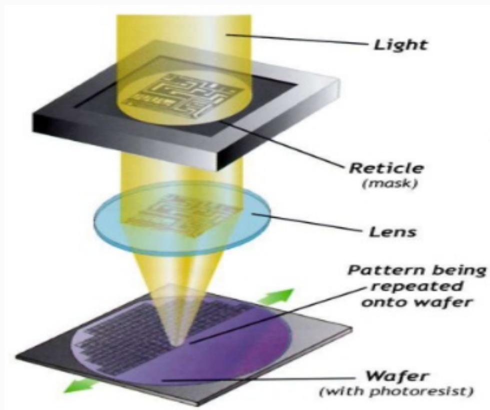
- Sensor and readout electronics are separate entities
  - Separate optimization for high rate
- Charge collection by **drift in depleted bulk**
  - Large signal, rad-hard, fast charge collection
- Complex readout in ASICs
  - Zero-suppression and in-pixel hit buffering
  - **Time resolution O(ns)**
- Moderate spatial resolution **O(10-100 µm)**
- **High material** budget, **few %X0**
  - Power hungry devices
- **High cost**
  - Sensor and hybridization

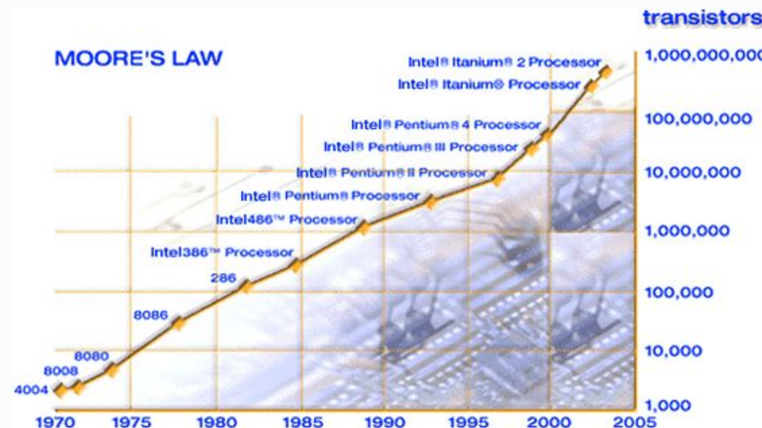




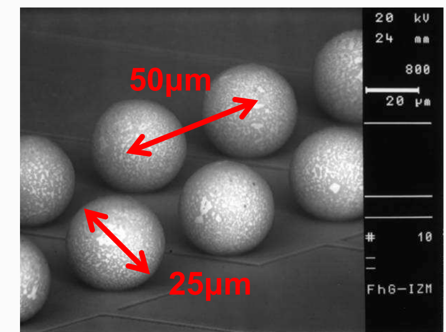
Technology enablers for hybrid pixels

- The development of **IC technologies for the consumer electronics market** in the 90s enabled the development of pixel detectors for the LHC
  - Planar process and **photolithography**
  - **VLSI** (Very Large Scale Integration) in **deep submicron CMOS technologies**
  - Fine pitch **bump bonding** and **flip chip**



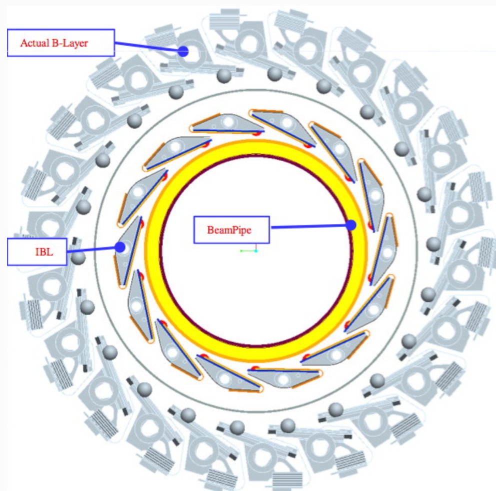


Bump bonds on ATLAS FE-I3 wafer

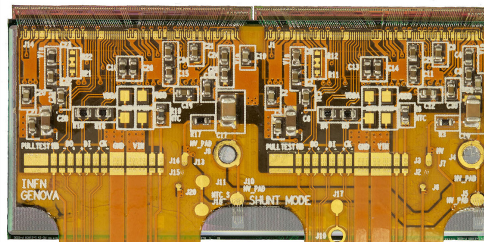


The ATLAS Insertable B-Layer detector

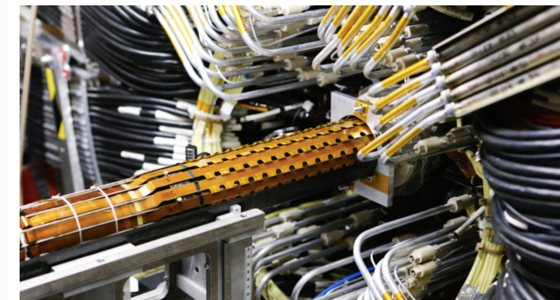
- 4th ATLAS pixel detector layer inserted at **33.5 mm radius** in 2013-2014
  - Maintain and improve robustness and performance of tracking and vertexing during the LHC Phase 1
- New sensor and electronic technologies radiation tolerant up to **5E15 n_{eq}/cm^2** and **250 Mrad**
- Lightweight detector design: **1.88% X0**
  - Low mass module design, low density carbon foam support structures, CO_2 evaporative cooling, aluminium conductor for power cables



IBL planar sensor module

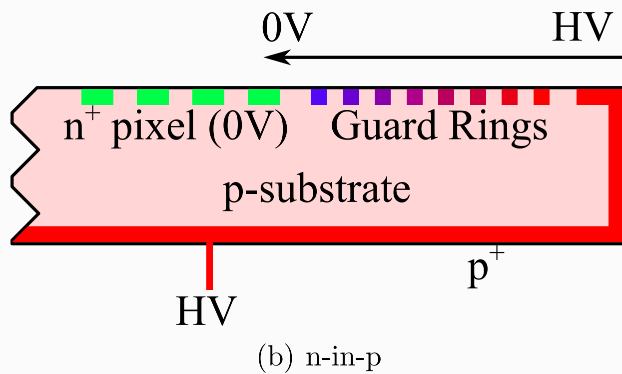


50 x 250 μm^2 pixel pitch
200 µm thin sensor
150 µm thin ASIC



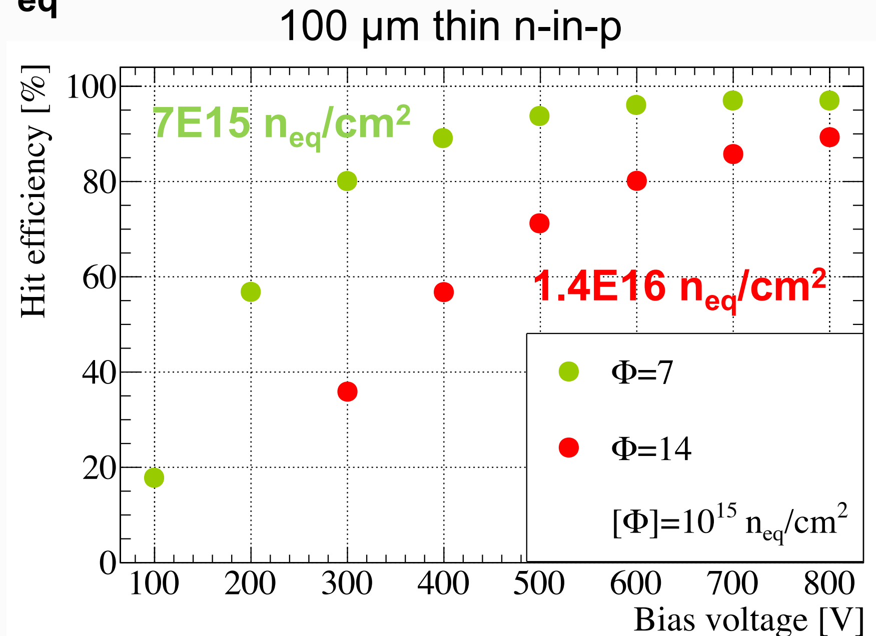
Planar sensors for high luminosity

- Sensor designed optimized to guarantee high E-field, short drift distance and fast charge collection after fluence up to **1E16 n_{eq}/cm^2**
  - Minimize trapping due to radiation-induced defects in silicon bulk
- Thin sensors (**100-150 µm**) with optimized edge region and guard rings structure withstanding **V_{bias} up to 1 kV**
  - Improved breakdown behavior after irradiations
- Hit efficiency above 90% at **1E16 n_{eq}/cm^2**



(b) n-in-p

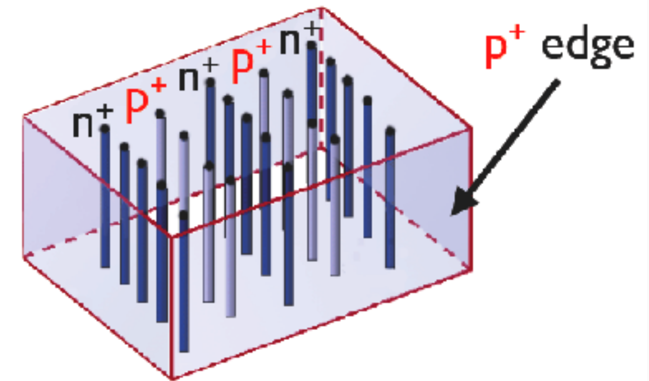
100 µm thin n-in-p

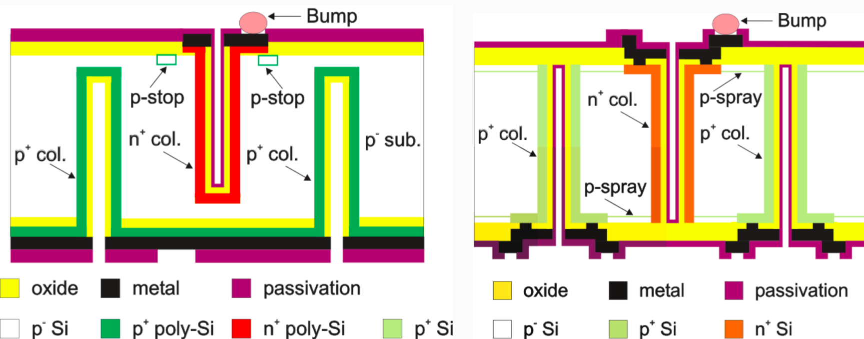


S. Terzo, https://publications.mppmu.mpg.de/2015/MPP-2015-291/FullText.pdf

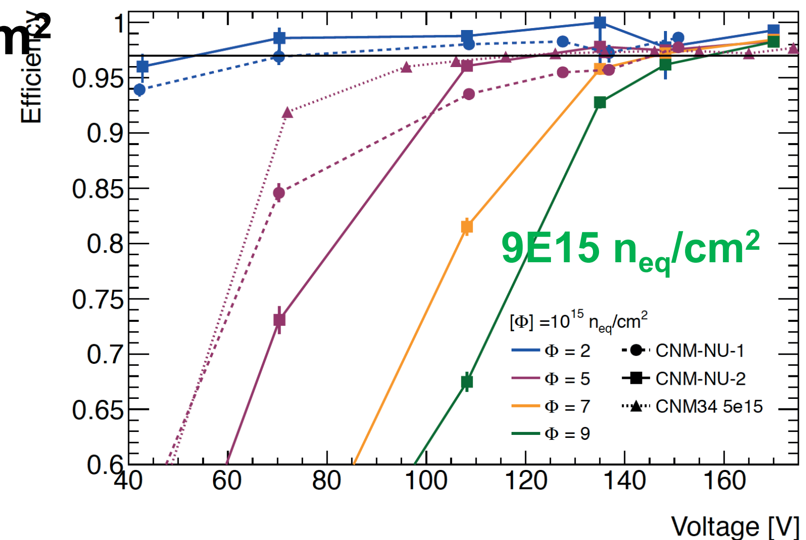
3D sensors for high luminosity

- First application in the IBL detector
- Geometrical radiation tolerance
- Particle path different from drift path
- **High field with low voltage**
  - Short charge collection distance (30-50 µm)
  - Fast response
- Hit efficiency of **~99%** at **~1E16 n_{eq}/cm^2** with **V_{bias} <200 V**





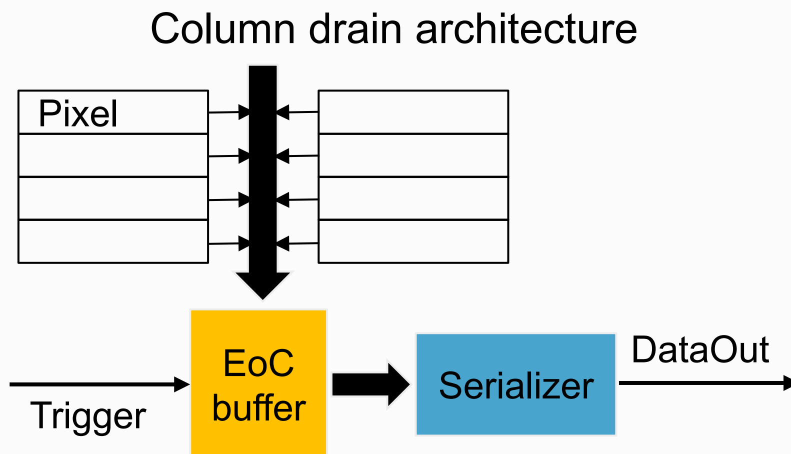
CERN-LHCC-2010-013, ATLAS TDR 19

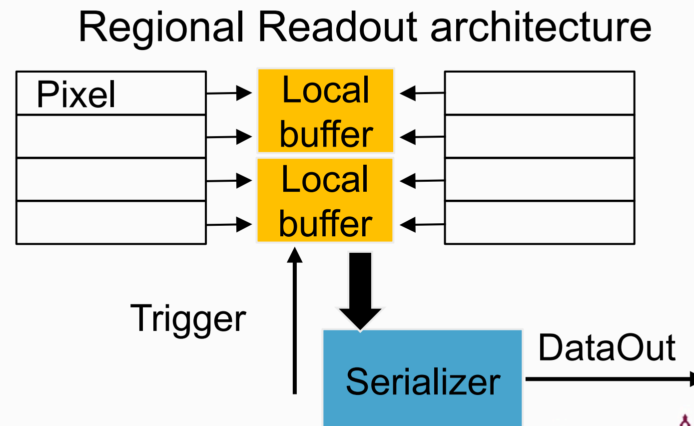


J. Lange et al., 2011 JINST 11 C11024

Evolution of readout architecture

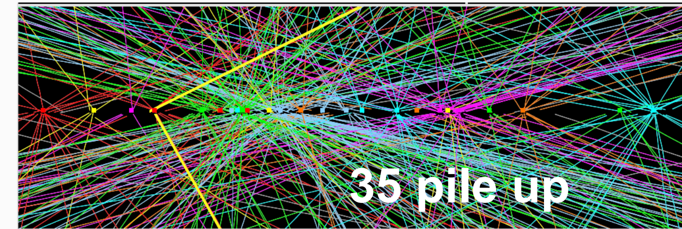
- Early generation of pixel readout chips (ATLAS FE-I3) was based on **column drain architecture**
- This architecture become inefficient at the IBL radius above nominal LHC luminosity → congestion in double column (DC) readout bus
- Store hits locally and move only if triggered → **regional readout architecture** (ATLAS FE-I4)
  - Reflects the **cluster nature of physics hits**
  - Groups of 2x2 pixels share digital logic, i.e. memory and time information → **cluster charge stored with less information**

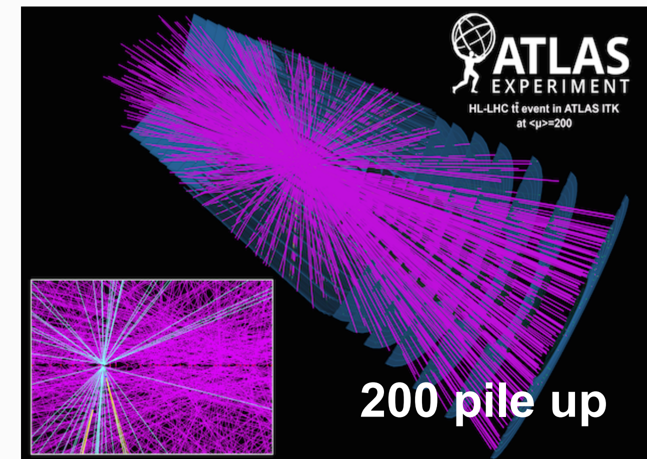


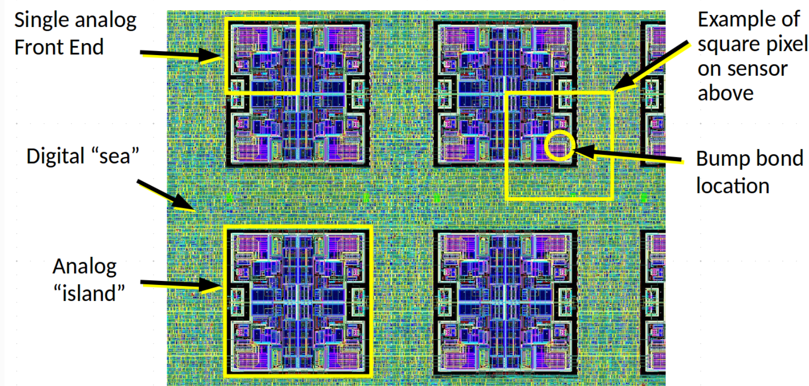


Readout for HL-LHC innermost layers

- Analog "islands" in a digital synthesized "sea"
- Collection of large **digital cores** containing many regions
  - Complex functionality in the pixel matrix
  - Resources shared among many pixels
- **2 dimensional digital connectivity**
- Smart clustering in the pixel matrix to send most information with least bandwidth



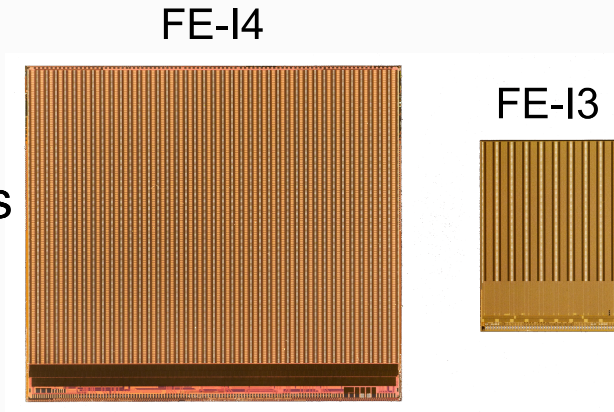




N. Wermes, https://indico.cern.ch/event/556692/

RD-53

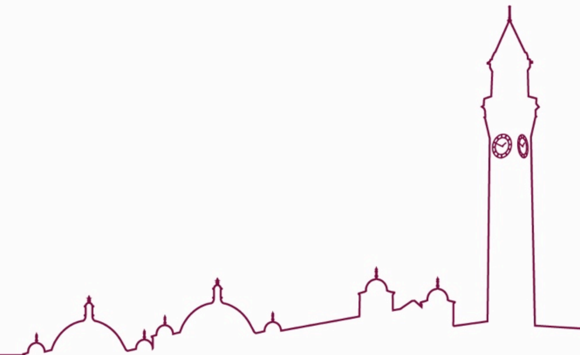
FE-I3, FE-I4, FE65



- Availability of smaller CMOS technology nodes
  - Higher logic density (more memory/unit area)
  - Smaller pixels
  - Higher throughput
  - Radiation hardness (technology & layout)

	FE-I3 LHC Run 1	FE-I4 LHC run 2 & 3	FE65 HL-LHC Run 4-5
Tech node	**250nm**	**130nm**	**65nm**
Chip size [mm^2]	7.4 x 11	18.8 x 20.2	> 20 x 20
# transistors	3.5M	87M	1G
Hit rate [Hz/cm^2]	**100M**	**400M**	**2G**
Output bandwidth	**40 – 60 Mb/s**	**0.3 – 1.2 Mb/s**	**2 – 20 Gb/s**
Pixel size [μm^2]	400 x 50	250 x 50	50 x 50
# readout channels	18 x 160	336 x 80	TBD
TID [rad]	**100M**	**200M**	**1G**

State-of-the art pixel detectors:
Monolithic Active Pixel Sensors (MAPS)

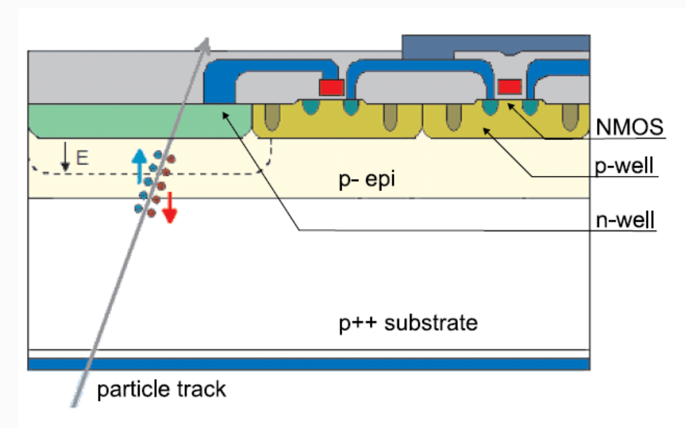


Monolithic Active Pixel Sensors

- Sensor and electronics are implemented in the same silicon substrate
  - **Modified CMOS process**

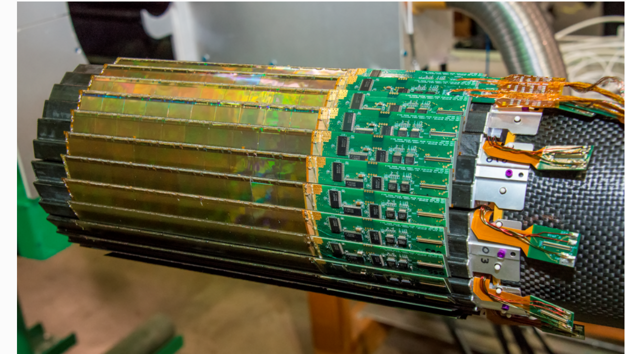
- Charge collection primarily by **diffusion** in the **epitaxial layer**
  - Small signal, moderate radiation hardness, slow
- Simple readout architecture
  - Simple in-pixel circuitry and limited hit storage
  - **Time resolution = O(μs)**

- High spatial resolution **O(1-5 μm)**
- Low material budget, **< 0.5% X0**
  - Low power
- **Lower cost**
  - Commercial process

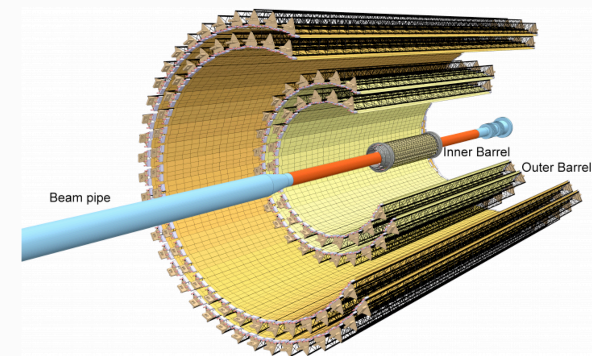


MAPS in HI experiments

- The first use of MAPS detectors in physics experiments was at **STAR** Heavy Flavour Tacker (HFT) at RHIC
  - Detector area = **0.15 m^2**
  - **ULTIMATE-2** sensor
  - Data taking since 2014

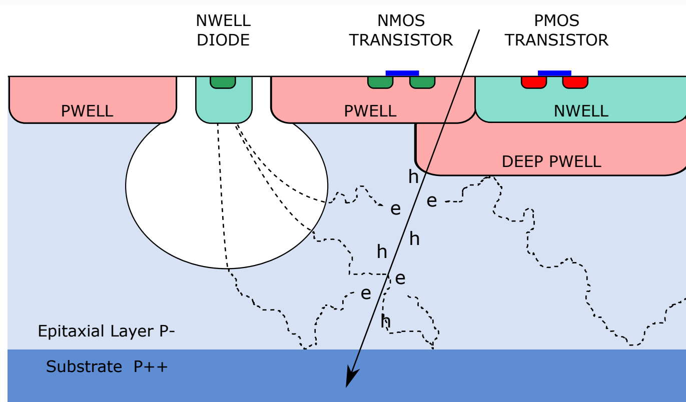


- MAPS have been chosen for the **ALICE** Inner Tracking System (ITS) upgrade at LHC
  - Detector area = **12 m^2**
  - **ALPIDE** sensor
  - Data taking to start in 2020

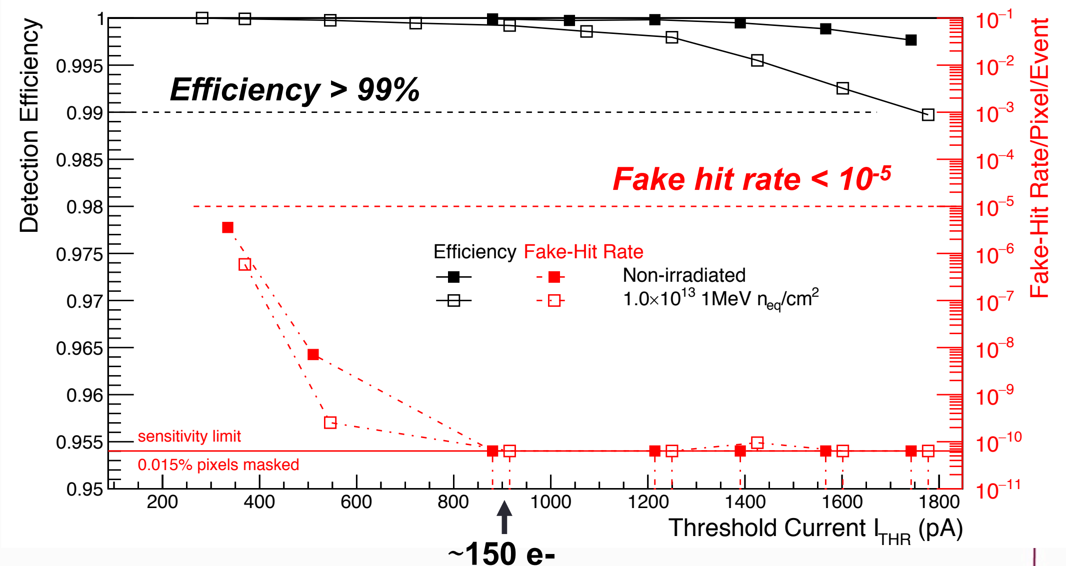


ALPIDE sensor for ALICE ITS

- TowerJazz 180nm CMOS imaging process
- Partial depletion at V_{bias} = 6V, but charge collection still mostly by diffusion
- **Efficiency > 99.5%** and **fake hit rate < 10^{-5}** over wide threshold range up to **1e13 (1MeV n_{eq})/cm^2**

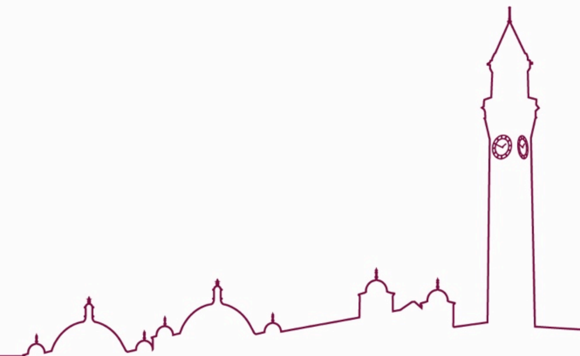


28 x 28 μm^2 pixel pitch
25 μm epi-layer, 1 kOhm cm
<2 μs time resolution

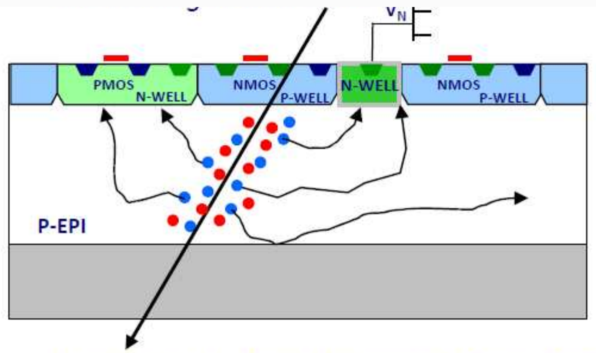


G. Aglieri Rinella, NIMA 845 (2017) 583–587

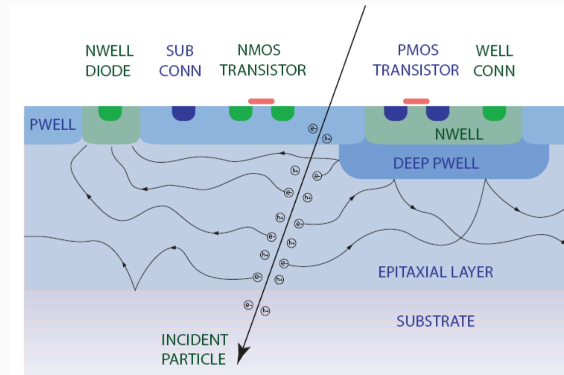
New developments:
Depleted MAPS



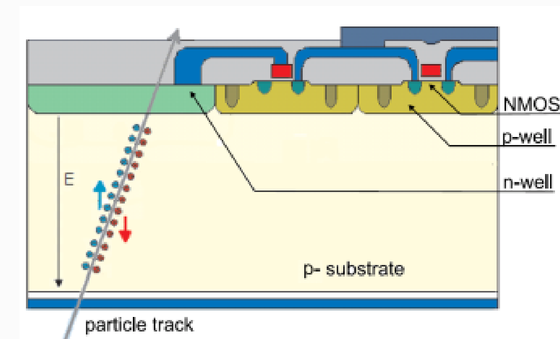
MAPS evolution



IHEP Strasburg

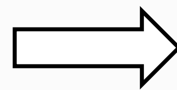


RAL



KIT, Bonn

No depletion
NMOS only



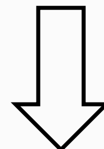
No depletion
full CMOS

Depletion
full CMOS

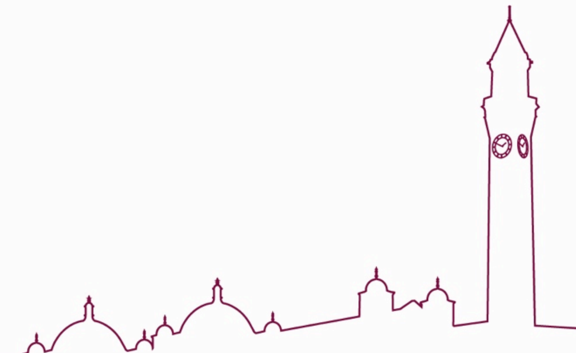
Deep implants /nested well

High Resistivity (HR) substrates
High Voltage (HV) transistors

+ backside processing

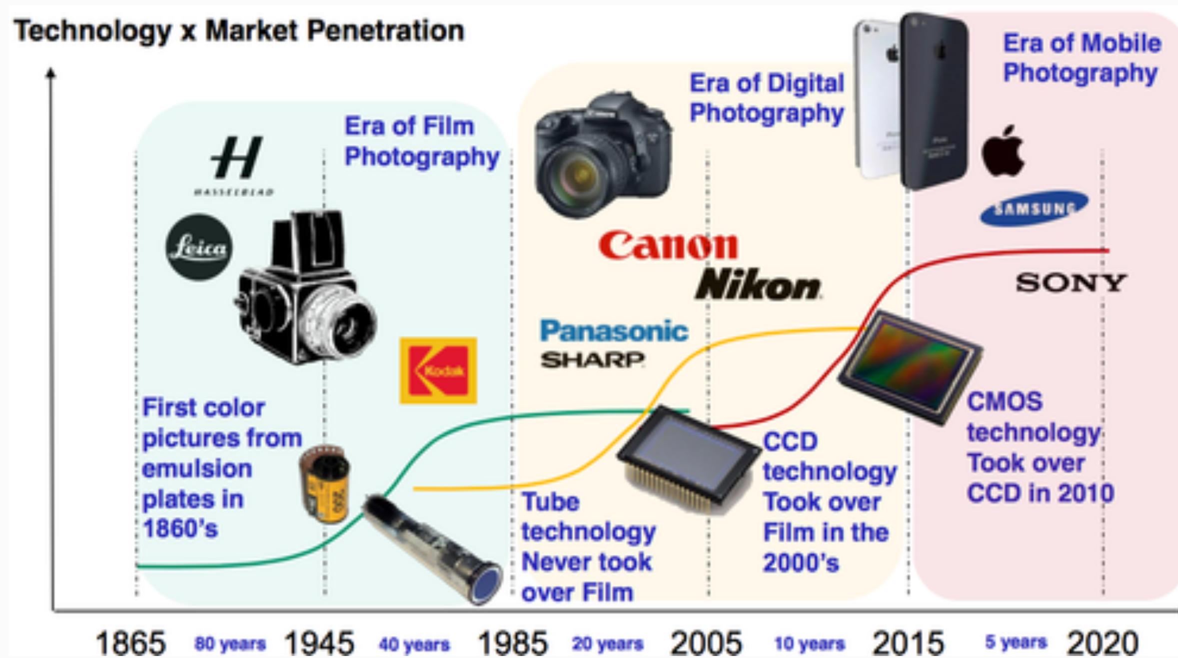


Depleted MAPS



CMOS imaging technologies

- The **camera phone market** pushed the development of CMOS imaging technologies since the 90s
- Wrt. CCDs, CMOS imaging sensors have **low power, and more integrated logic functionalities**



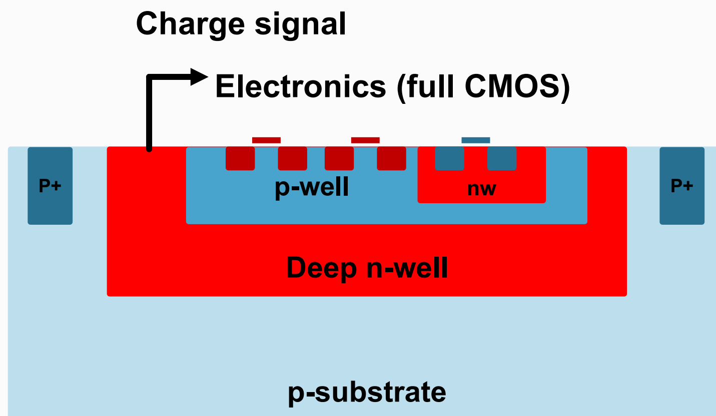
https://www.eetimes.com/document.asp?doc_id=1325655&image_number=1

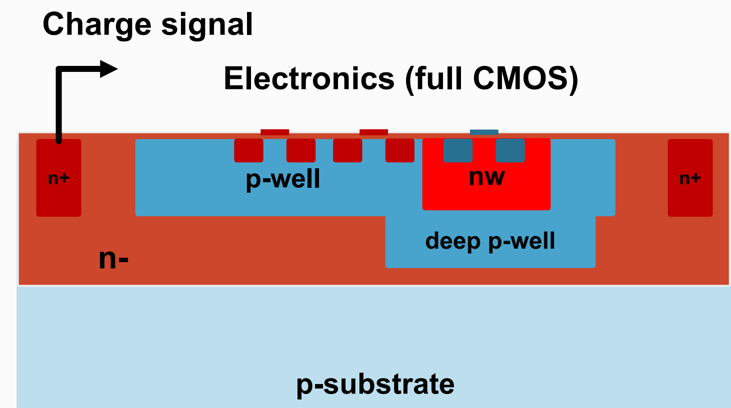
Technology overview

Commercial CMOS technologies featuring **high voltage** capabilities and/or **high resistive substrate**

DMAPS layout options

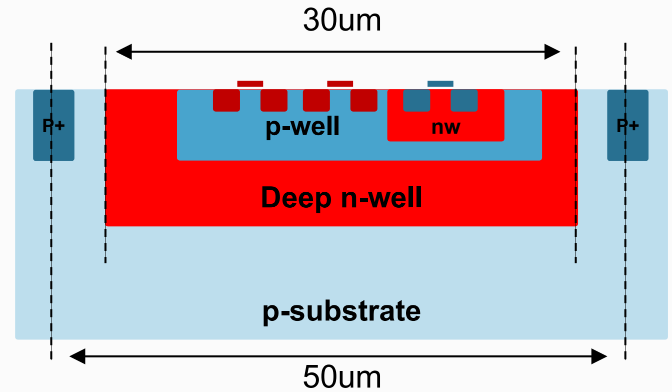
- Large collection electrode
  - Electronics inside the collection electrode
  - Large sensor C → higher power, higher noise
  - Full CMOS w/ isolation between NW and DNW (quadrupole well process)
- Small collection electrode
  - Electronics outside the collection electrode
  - **Full depletion with additional n implant**
  - **Small sensor C → low power, low noise**
  - Full CMOS with additional deep p-well (triple well process)



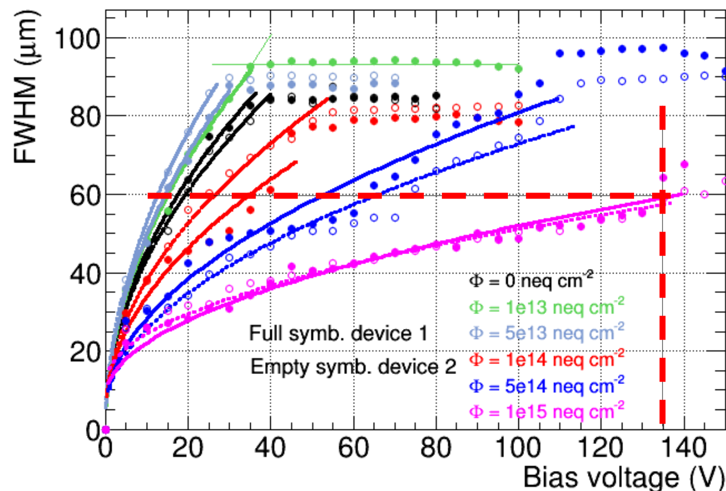


Large collection electrode with LFoundry

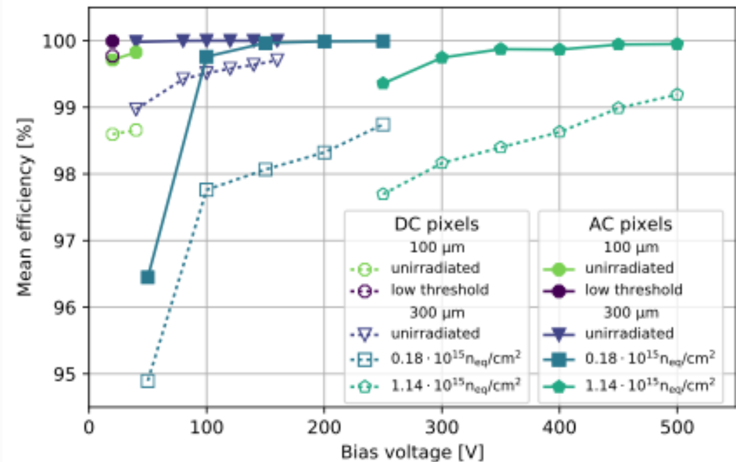
- LFoundry 150 nm CMOS process
- Depletion at **1E15 n_{eq}/cm^2 ~50-60 μm** depletion
- Hit-efficiency measured in test beam is above **99.9%** after **1E15 n_{eq}/cm^2**



50 x 250 μm² pixel pitch
100 μm HR substrate, 2-4 kOhm cm



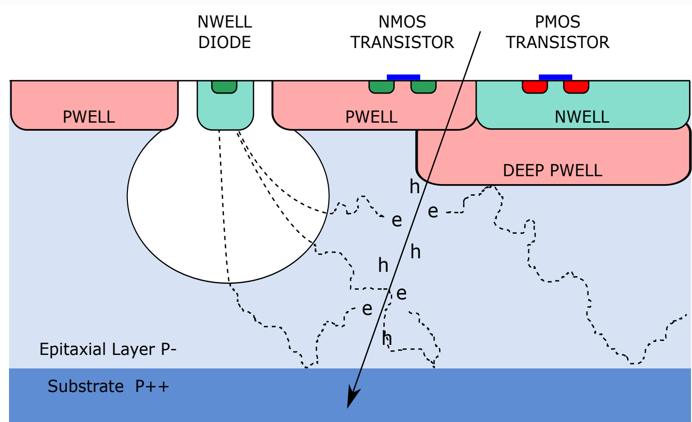
I. Mandic et al., 2017 JINST 12 P02021



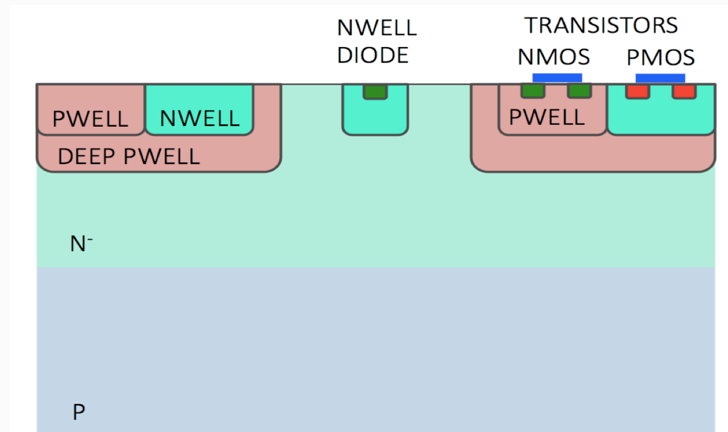
D.-L. Pohl, 2017 JINST 12 P06020

Small collection electrode with TJ

- Modified TowerJazz 180nm CMOS imaging process
- Recent development by CERN/TJ* to improve the radiation hardness of the TJ 180nm CMOS process
- Deep planar junction in epi layer to allow **lateral depletion** below the electronics



Standard process



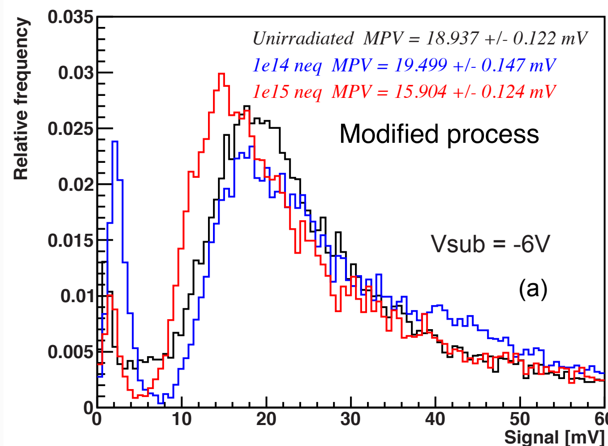
Modified process

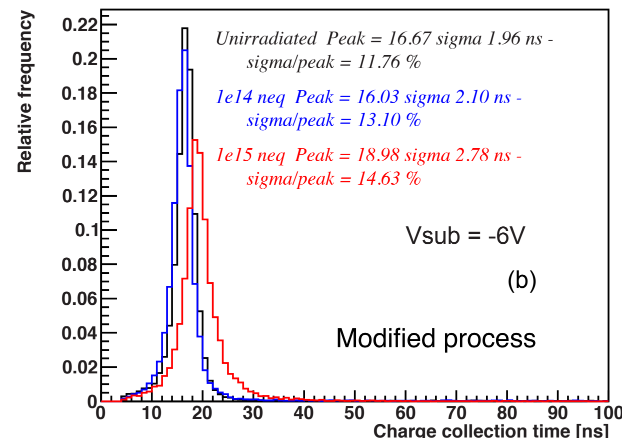
*W. Snoeys et al, NIMA 871 (2017) 90–96

TJ modified process

- **Signal size unchanged** after neutron irradiation to **1E15 n_{eq}/cm^2**
  - No signal after 1E14 n_{eq}/cm^2 in standard process

- Spread in charge collection time at 1E15 n_{eq}/cm^2 lower than for standard process before irradiation, **2.78ns vs 4.6ns**





50 x 50 μm² pixel pitch
25 μm epi-layer

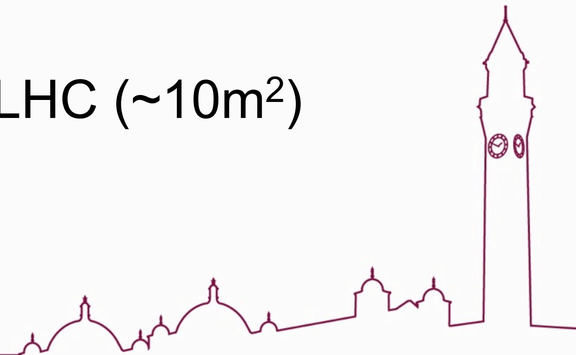
Depletion reaches lateral regions and charge is collected by drift

H. Pernegger et al., 2017 JINST 12 P06008

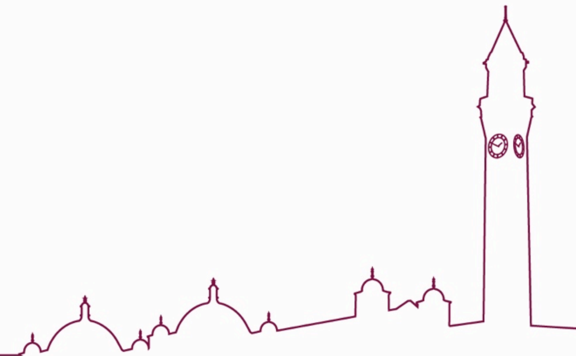
Advantages of depleted MAPS

- Commercial technologies
  - **Low cost**
  - High throughput
  - Multiple vendors
- Simplified module concept
  - **Ease of construction**
- **Thin sensing layer** (20-100 μm)
  - Possible constant charge collection volume with dose
  - Reduce cluster size at large eta
- Charge collection by drift and full CMOS electronics (but not yet outperforming hybrid pixels!)

→ Candidate for **outer pixel layers** at the HL-LHC (~10m^2)

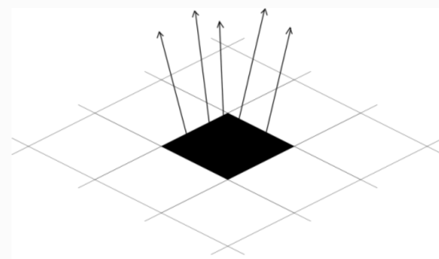


New developments:
Digital electromagnetic calorimetry with DMAPS at future colliders

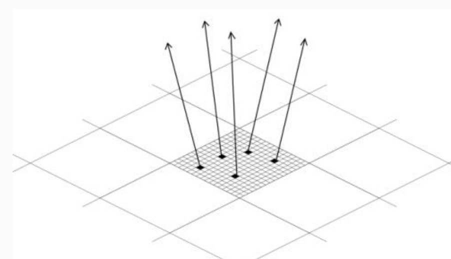


Digital Calorimetry with MAPS

- Dates back to ~2005 work within CALICE for **linear colliders**
  - See work with TPAC, FORTIS, and CHERWELL sensors
- Make a pixelated calorimeter to count the number of particles in each sampling layer to **reduce uncertainties due to Landau fluctuations of energy deposits**
- **Small pixels** to avoid undercounting and non-linear response in high particle density environments
- Proposed ILD ECAL has a silicon area of ~2400m^2. Digital variant would require 10^{12} pixels. Requires **low cost, ease of construction, low power**



Analogue: 5mm pitch



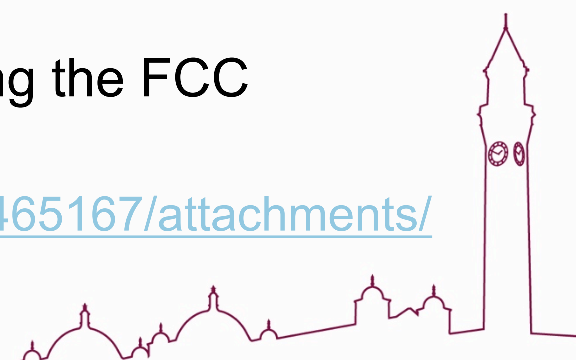
Digital: 50um pitch

DECAL for FCC-hh

- DECAL for hadron colliders will have additional complexities such as pile-up, much higher energy jets, higher radiation environment → **DMAPS**

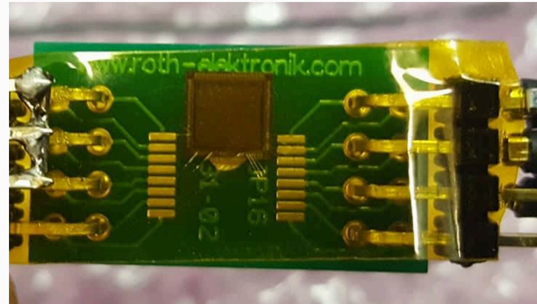
- **Reconfigurable, radiation hard DMAPS** for outer tracking and calorimetry
  - Birmingham, RAL (PPD & TD), Sussex
  - Targeting 1E15 n_{eq}/cm^2 (ECAL barrel region at FCC-hh)
  - Complementary technology as a pre-shower / outer tracker
  - Seamless transition from outer tracker to ECAL possible with same technology

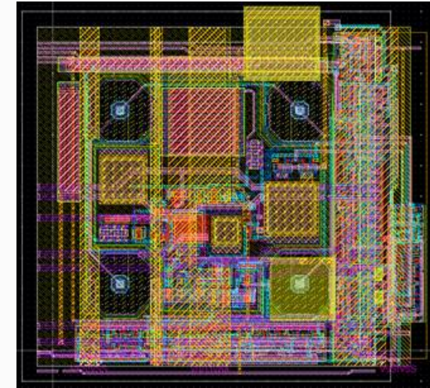
- Chip design informed by detector simulations using the FCC simulation software
  - https://indico.cern.ch/event/556692/contributions/2465167/attachments/1469036/2272313/pricet_decal_fccweek2017.pdf



DECAL chip development

- Specs
  - 50 x 50 μm^2 pixels
  - 4 collection electrodes/pixel
  - 25 ns readout
  - 64 x 64 pixel matrix, 5 mm^2

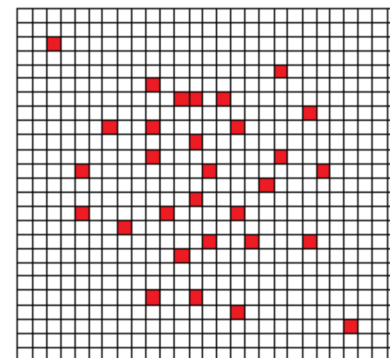


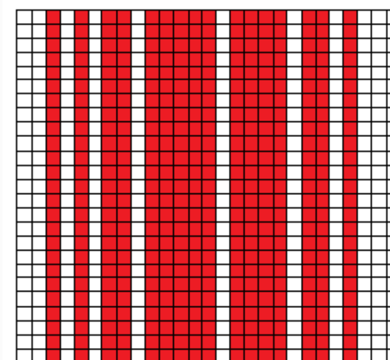


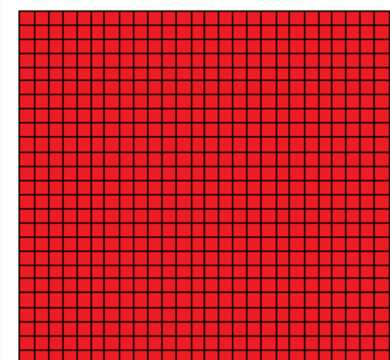
- Submission
  - The **DECAL chip** was submitted in May in the **standard TJ process**, testing started a couple of weeks ago
  - **Test structures** have been submitted in the **modified TJ process** in September
- Radiation hardness
  - Target radiation hardness to be demonstrated with passive test structures in the TJ modified process
  - Radiation-hardness of DECAL chip in standard process possibly enhanced by multiple collection electrode configuration

Reconfigurability

- Pixel mode
  - Read out address for every pixel that fires
  - Not available in this iteration
- Column mode
  - Read out hit column addresses, and up to 3 hits/column
  - Flag set if >3 hits/column
  - Outer tracking and possibly pre-shower
- Pad mode
  - Sum the number of hit pixels in a 5x5mm^2 pad and readout this value
  - Reduced number readout channels and data rate by not reading every hit pixel address in 25ns but combining information in each 5x5mm^2 pad using fast logic
  - Calorimetry

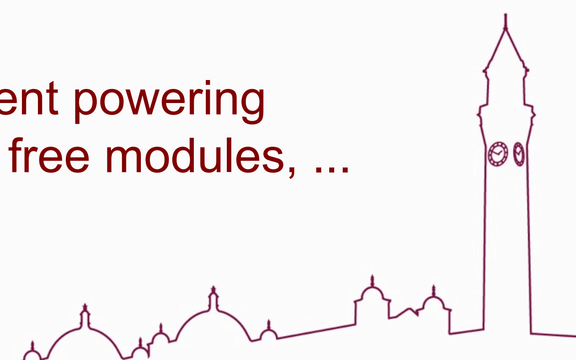






Conclusion

- Pixel detectors are the technology of choice for tracking and vertexing
- Different concepts have been developed to cover both high rate and high precision demands from different experiments
- Development of monolithic pixel detectors with commercial CMOS technologies is bringing together the advantages of both hybrid and MAPS detectors and offers an attractive low cost solution for future large area tracking detectors and calorimeters
- Many more developments ongoing…
  - Diamon sensors, 4D detectors, low mass and efficient powering schemes, lightweight support structures, wire-bond free modules, ...



Backup